POWER MANAGEMENT

OUTLINES

- Local Power Management Aspects
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
  - Battery
  - DC – DC Converter
- Dynamic Power Management
  - Dynamic Operation Modes
  - Transition Costs
  - Dynamic Scaling
  - Task Scheduling
- Conceptual Architecture
  - Architectural Overview

POWER MANAGEMENT

The power consumption of a wireless sensor network (WSN) is of crucial concern because of the scarcity of energy. Whereas energy is a scarce resource in every wireless device, the problem in WSNs is amplified for the following reasons:

1. The *nodes are very small in size* to accommodate high-capacity power supplies compared to the complexity of the task they carry out.
2. It is *impossible to manually change*, replace, or recharge batteries – WSNs consist of a large number of nodes.
3. *The size of nodes* is still a *constraining* factor for renewable energy and *self-recharging mechanisms*.
4. *The failure of a few nodes* may cause the entire network to fragment prematurely.

POWER MANAGEMENT

- The problem of power consumption can be approached from *two angles*:
  - Develop energy-efficient communication protocols
    - self-organization, medium access, and routing protocols.
  - Identify activities in the networks that are both wasteful and unnecessary then mitigate their impact.

- Most inefficient activities are results of *non-optimal configurations* in hardware and software components:
  - e.g., a considerable amount of energy is wasted by an idle processing or a communication subsystem.
  - A radio that aimlessly senses the media or overhears while neighboring nodes communicate with each other consumes a significant amount of power.

POWER MANAGEMENT

Wasteful and unnecessary activities can be described as *local* or *global*":

- *e.g.,* some nodes exhausted their batteries prematurely because of *unexpected overhearing* of traffic that caused the communication subsystem to become operational for a longer time than originally intended.

- some nodes exhausted their batteries prematurely because they aimlessly *attempted to establish links with a network* that had become no longer accessible to them.

POWER MANAGEMENT

A *dynamic power management (DPM)* strategy ensures that power is consumed economically

- The strategy can have a *local* or *global* scope, or *both*
- *A local DPM strategy* aims to
  - Minimize the power consumption of *individual nodes*
    - by providing each subsystem with the amount of power that is sufficient to carry out a task at hand
    - when there is no task to be processed, the DPM strategy forces some of the subsystems to operate at the *most economical power mode* or puts them into a *sleeping mode*"

- *A global DPM strategy* attempts to
  - Minimize the power consumption of *the overall network* by defining a *network-wide sleeping state*

POWER MANAGEMENT

- *Synchronous sleeping schedule*
  - Let individual nodes *define* their own sleeping schedules
  - *Share* these schedules with their neighbors to enable a coordinated

    sensing and an efficient inter-node communication
  - The *problem* is that neighbors need to synchronize time as well as

    schedules and the process is energy intensive
- *Asynchronous sleeping schedule*
  - Let individual nodes *keep* their sleeping schedules to themselves
  - A node that initiates a communication should *send a preamble* until it

    receives an acknowledgment from its receiving partner
  - Avoids the needs to synchronize schedules
  - It can have *a latency side-effect* on data transmission

POWER MANAGEMENT

- In both approaches, individual nodes *wake up periodically*:
  - to determine whether there is a node that wishes to communicate with them
  - to process tasks waiting in a queue
- Fundamental premises about Embedded systems:
  - predominantly event-driven
  - experience non-uniform workload during operation time
- DPM refers to *selectively shutting-off* and/or *slowing-down* system components that are idle or underutilised
- A policy determines the type and timing of power transitions based on *system history*, *workload* and *performance constraints*

LOCAL POWER MANAGEMENT ASPECTS

The first step is the *understanding of how power is consumed* by the different subsystems of a wireless sensor node:

- Wasteful activities to be avoided and to frugally budget power
- One to estimate the overall power dissipation rate in a node and how this rate affects the lifetime of the entire network
- In the following subsections, a mode detail observation into the different subsystems of a node is made:
  - Processor Subsystem
  - Communication Subsystem
  - Bus Frequency and RAM Timing
  - Active Memory
  - Power Subsystem
    - Battery
    - DC – DC Converter

POWER SUBSYSTEM

- Most existing processing subsystems employ microcontrollers, notably
  - Intel's StrongARM and Atmel's AVR
- These microcontrollers can be configured to operate at *various power modes"*
  - *e. g.,* the ATmega128L microcontroller has *six different power modes*:
    - Idle,
    - ADC noise reduction,
    - Power save,
    - Power down,
    - Standby, and
    - Extended standby.

POWER SUBSYSTEM

Sleep Mode	Active clock domains					Oscillators		Wake up sources					
	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT7	TWI Addr. Match	Timer	EEPROM Ready	ADC	Other I/O
Idle			X	X	X	X	X	X	X	X	X	X	X
ADC noise red.				X	X	X	X	X	X	X	X	X	
power down								X	X				
Power save					x		x	x	x	x			
standby						x		x	x				
Ext. standby						x	x	x	x	x			

- The *idle* mode stops the CPU
  - While allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning.
- The *power down* mode saves the registers' content
  - While freezing the oscillator and disabling all other chip functions until the next interrupt or Hardware Reset.

POWER SUBSYSTEM

- In the *power-save* mode, the asynchronous timer continues to run
  - Allowing the user to maintain a timer base while the remaining components of the device enter into a sleep mode
- The *ADC noise reduction* mode stops the CPU and all I/O modules
  - *Except* the asynchronous *timer* and the *ADC*
  - The aim is to minimize switching noise during ADC conversions
- In *standby* mode, a crystal/resonator oscillator runs while the remaining

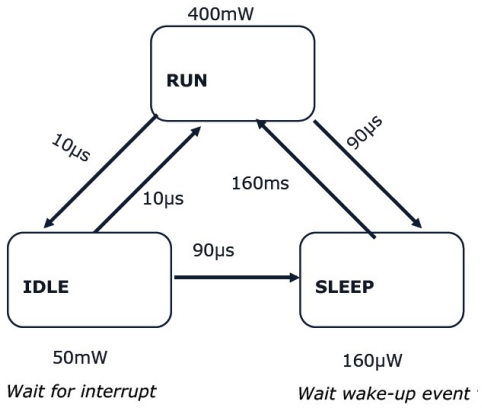
  hardware components enter into a sleep mode
  - This allows very fast start-up combined with low power consumption
- In *extended standby* mode, both the main oscillator and the asynchronous

  timer continue to operate

POWER SUBSYSTEM

- Additional to the above configurations, the processing subsystem can *operate* with *different supply voltages* and *clock frequencies.*
- *Transiting* from one power mode to another also has its own power and latency cost.

Power state machine for the StrongARM-1100 processor



COMMUNICATION SUBSYSTEM

- The *power consumption* of the communication subsystem can *be influenced*

  by several aspects:
  - the modulation type and index
  - the transmitter's power amplifier and antenna efficiency
  - the transmission range and rate
  - the sensitivity of the receiver

- These aspects can be *dynamically reconfigured*

COMMUNICATION SUBSYSTEM

Determining the most efficient active state operational mode is *not a simple decision*

- *e.g.,* the power consumption of a transmitter may *not* necessarily be reduced by simply reducing the transmission rate or the transmission power!
  - the reason is that there is a *tradeoff* between *the useful power required for data transmission* and the *power dissipated in the form of heat* at the power amplifier
- usually, the dissipation power (heat energy) *increases* as the transmission power *decreases*
- in fact most commercially available transmitters operate efficiently at one or two transmission power levels
  - below a certain level, the efficiency of the power amplifier *falls drastically*

COMMUNICATION SUBSYSTEM

- In some cheap transceivers, even when at the maximum transmission power mode, more than ***60%*** of the supply DC power is dissipated in the form of useless ***heat***.
- For example, the ***Chipcon*** *CC2420* transceiver has eight programmable output power levels ranging from −24 dBm to 0 dBm.

Chipcon CC2420: Output power settings and typical current consumption at 2.45 GHz

PA level	Output power dBm	Output power mW	Current consumption mA	Power consumption* mW
31	0	1	17.4	31.32
27	−1	0.794328235	16.5	29.7
23	−3	0.501187234	15.2	27.36
19	−5	0.316227766	13.9	25.02
15	−7	0.199526231	12.5	22.5
11	−10	0.1	11.2	20.16
7	−15	0.031622777	9.9	17.82
3	−25	0.003162278	8.5	15.3

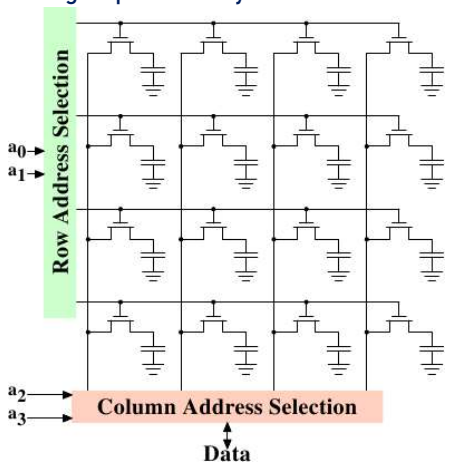
*$V_{dd} = 1.8$ V

BUS FREQUENCY AND RAM TIMING

- The processor subsystem consumes power when it interacts with the other subsystems via *the internal high speed buses*.
- The specific amount depends on the *frequency* and *bandwidth* of the communication.
- These two parameters can be optimally configured depending on the *interaction type*, but *bus protocol timings* are usually optimized for particular bus frequencies.
- Moreover, bus controller drivers require to be notified *when bus frequencies change* to ensure optimal performance.

ACTIVE MEMORY

- It is made up of *capacitor-transistor pairs (DRAM)*
  - arranged in rows and columns, each row being a single memory bank
  - have to be recharged periodically in order to store data



ACTIVE MEMORY

- The *refresh interval*:
  - a measure of the number of rows that must be refreshed
  - a *low refresh interval* corresponds to a *high clock frequency*
  - a *higher refresh interval* corresponds to a *low clock frequency*
- Consider two typical values: 2K and 4K
  - 2K: *refreshes more cells* at a low interval and completes the process faster, thus it *consumes more power*
  - 4K: *refreshes less cells* at a slower frequency, but it *consumes less power*
- A DRAM memory unit can be configured to operate in one of the following *power modes*:
  - temperature-compensated self-refresh mode
  - partial array self-refresh mode
  - power down mode

ACTIVE MEMORY

- *Temperature-compensated self-refresh mode*
  - the standard refresh rate of a memory unit can be adjusted according to its ambient *temperature.*
- *Partial array self-refresh mode*
  - the self-refresh rate can be *increased* if the entire memory array is not needed to store data
  - the refresh operation can be *limited* to the portion of the memory array in which data will be stored
- *Power down mode*
  - if no actual data storage is required, the supply voltage of most or the entire on-board memory array can be *switched off*

ACTIVE MEMORY

The *RAM timing* is another parameter that affects the power consumption of the memory unit

- it refers to the *latency* associated with accessing the memory unit
- before a processor subsystem accesses a particular cell in a memory, it should first *determine* the particular *row or bank*
- then *activate* the row with a *row access strobe (RAS)* signal
- the activated row can be accessed until the data is exhausted
- the time required to activate a row in a memory is t_{RAS}, which is relatively small but could *impact the system's stability* if set incorrectly

ACTIVE MEMORY

The *delays* between the activation of a row (a cell) and the writing of data into or reading of data from the cell is given as $t_{RCD.}$

- This time can be short or long, depending on how the memory cell is accessed.
- If it is accessed sequentially, it is insignificant.
- If it is accessed in a random fashion, the current active row must first be *deactivated* before a new row is activated.
- In this case, t_{RCD} can cause significant *latency.*

ACTIVE MEMORY

A memory cell is activated through a *column access strobe (CAS)*

- The delay between the CAS signal and the availability of valid data on the data pins is called *CAS latency.*
- *Low CAS latency* means *high performance* but also *high power consumption.*
- The time required to terminate one row access and begin the next row access is t_{RP}.
- The time required to switch rows and select the next cell for reading, writing, or refreshing is expressed as $t_{RP} + t_{RCD}$.
- The duration of time required between the active and precharge commands is called t_{RAS}.
- It is a measure of how long the processor must wait before the next memory access can begin.

ACTIVE MEMORY

Parameters of RAM timing

Parameter	Description
RAS	Row Address Strobe or Row Address Select
CAS	Column Address Strobe or Column Address Select
t_{RAS}	A time delay between the precharge and activation of a row
t_{RCD}	The time required between RAS and CAS access
t_{CL}	CAS latency
t_{RP}	The time required to switch from one row to the next row
t_{CLK}	The duration of a clock cycle
Command rate	The delay between Chip Select (CS)
Latency	The total time required before data can be written to or read from memory

When a RAM is accessed by *clocked logic*, the times are generally rounded up to the *nearest clock cycle*

- for example, when accessed by a 100-MHz processor (with 10 ns clock duration), a 50-ns SDRAM can perform the first read in 5 clock cycles and additional reads within the same page every 2 clock cycles.
- this is generally described as "5 – 2 – 2 – 2" timing.

POWER SUBSYSTEMS

- The power subsystem supplies power to all the other subsystems
- It consists of:
  - ***The battery***
  - ***The DC – DC converter***
    - It provides the right amount of supply voltage to each individual hardware component
    - By transforming the main DC supply voltage into a suitable level
    - The transformation can be a *step-down (buck)*, a *step-up (boost)*, or an *inversion (flyback)* process, depending on the requirements of the individual subsystem

POWER SUBSYSTEMS

The battery

- A wireless sensor node is powered by *exhaustible batteries*
  - the main factor affect the quality of these batteries is *cost.*
- Batteries are specified by a rated current capacity, C, expressed in *ampere-hour*
  - This quantity describes the rate at which a battery discharges without significantly affecting the prescribed supply voltage
  - As the discharge rate *increases*, the rated capacity *decreases*
  - Most portable batteries are rated at $1C$
    - This means a 1000 mAh battery provides 1000mA for 1 hour, if it is discharged at a rate of $1C$. *e.g.,*
      - ❖ at a rate of $0.5C$, providing 500mA for 2 hours.
      - ❖ at a rate of $2C$, 2000mA for 30 minutes.

POWER SUBSYSTEMS

The battery

In reality, batteries perform at *less than the prescribed rate*. Often, the *Peukert Equation* is applied to quantifying the capacity offset (i.e., how long a battery lasts in reality):

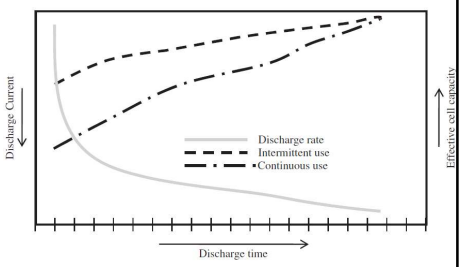
$$t = \frac{C}{I^n}$$

- Where C is the theoretical capacity of the battery expressed in ampere-hours
- I is the current drawn in Ampere (A)
- t is the time of discharge in seconds
- n is the Peukert number, a constant that directly relates to the internal resistance of the battery (A value close to 1 indicates that the battery performs well; the higher the number, the more capacity is lost when the battery is discharged at high current.)

POWER SUBSYSTEMS

Drawing current at a rate greater than the discharge rate results in a current consumption rate higher than the rate of diffusion of the active elements in the electrolyte. If this process continues for a long time, the electrodes run out of active material even though the electrolyte has not yet exhausted its active materials. This situation can be overcome by intermittently drawing current from the battery.

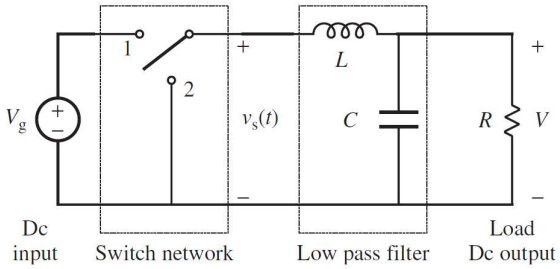
by intermittently using the battery, it is possible during quiescent periods to increase the diffusion and transport rates of active ingredients and to match up the depletion created by excessive discharge



because of this potential for recovery, the capacity reduction can be undermined and the operating efficiency can be enhanced

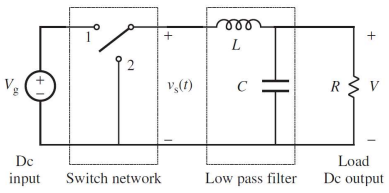
POWER SUBSYSTEMS

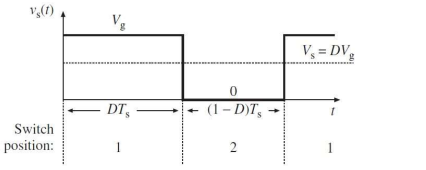
- The DC – DC converter transforms one voltage level into another
  - *The main problem* is its *conversion efficiency*
- A typical DC – DC convertor consists of
  - A power supply
  - A switching circuit
  - A filter circuit
  - A load resistor



A DC–DC converter consisting of a supply voltage, a switching circuit, a filter circuit, and a load resistance.

POWER SUBSYSTEMS





The output voltage of a switching circuit of a DC–DC converter

In the figure, the circuit consists of *a single-pole, double-throw (SPDT) switch*

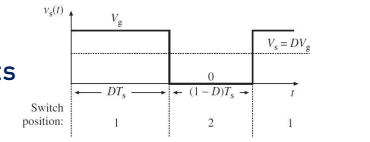
- SPDT is connected to a DC supply voltage, *Vg*.
- Considering the inductor, *L*, as a short circuit.
- The capacitor, *C*, as an open circuit for the DC supply voltage.
- The switch's output voltage, *Vs (t)* = *Vg* when the switch is in position 1.
- *s (t)* =0 When it is in position 2.
- Varying the position of the switch at a frequency, *fs* yields a periodically varying square wave, *vs (t),* that has a period *Ts =1/fs.*
- *vs (t)* can be expressed by a duty cycle *D.*
- *D* describes the fraction of time that the switch in position 1, (0 ≤ D ≤ 1).

POWER SUBSYSTEMS

- A DC – DC converter is realized
  - by employing active switching components
  - such as diodes and power MOSFETs
- Using the *inverse Fourier transformation*
  - The DC component of *vs (t)* (*Vs*) is described as:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\mathrm{d}t = DV_g$$

which is the average value of *vs (t)*.



The output voltage of a switching circuit of a DC–DC converter

- In other words, the integral value represents the area under the waveform of Figure for a single period, or the height of *Vg* multiplied by the time *Ts*.
- It can be seen that the switching circuit reduces the DC component of the supply voltage by a factor that equals to the duty cycle, *D* Since 0 ≤ *D*

POWER SUBSYSTEMS

The switching circuit consumes power

- Due to the existence of a resistive component in the switching circuit, there is power dissipation
- The efficiency of a typical switching circuit is between 70 and 90%
- In addition to the desired DC voltage, *vs (t)* also contains undesired harmonics of the switching frequency, *fs*
- These harmonics must be removed so that the converter's output voltage *v(t)* is essentially equal to the DC component *V= Vs*
- For this purpose, a DC – DC converter employs a *low pass filter*

POWER SUBSYSTEMS

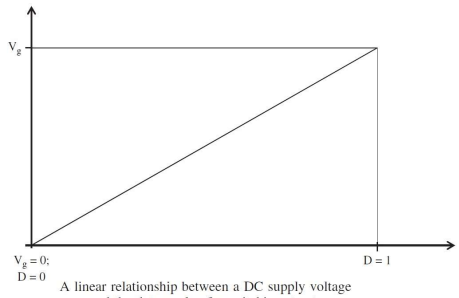
- In Figure, a first-order *LC* low pass filter is connected to the switching circuit
  - The filter's cutoff frequency is given by: $$f_c = \frac{1}{2\pi\sqrt{LC}}$$
  - The cutoff frequency, *fc*, should be sufficiently *less* than the switching frequency, *fs*
  - So that the low pass filter allows only the DC component of *vs (t)* to pass
- In an ideal filter, there is no power dissipation
  - Because the passive components (inductors and capacitors) are energy storage components
- Subsequently, the DC–DC converter produces a DC output voltage
  - Its magnitude is controlled by the duty cycle, *D*, using circuit elements that (ideally) do not dissipate power

POWER SUBSYSTEMS

- The conversion ratio, *M(D)*, is defined as the ratio of the DC output voltage, *V* , to the DC input voltage, *Vg*, under a steady-state condition:

$$M(D) = \frac{V}{V_g}$$

- For the buck converter shown in Figure, *M(D) = D*
- Figure illustrates the linear relationship between the input DC voltage, *Vg* and the switching circuit's duty cycle, *D.*

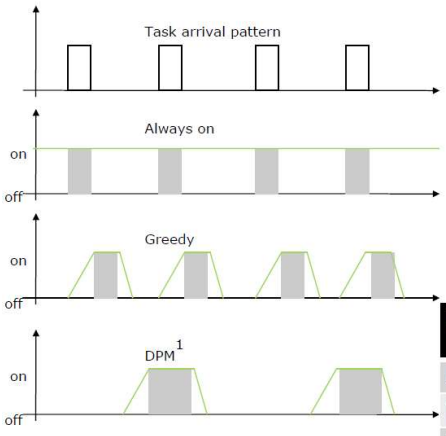


A linear relationship between a DC supply voltage and the duty cycle of a switching circuit.

DYNAMIC OPERATION MODES

- In general, a subcomponent or a part it can have *n* different power modes
  - If there are *x* hardware components that can have *n* distinct power consumption levels, a DPM strategy can define *x* × *n* différent power mode configurations, *Pn*.
- The *task* of the DPM strategy is:
  - select the optimal configuration that matches the activity of a wireless sensor node.
- Two associated *challenges*:
  - Transition between the different power configurations costs extra power.
  - A transition has an associated delay and the potential of missing the occurrence of an interesting event.

DYNAMIC OPERATION MODES

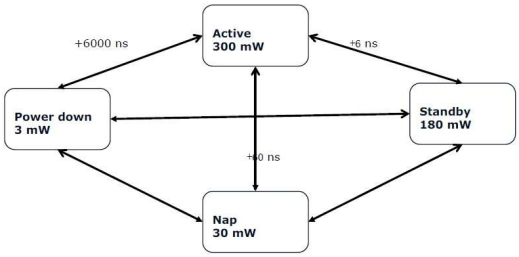


Parameter	Value
P_{on}	10 W
P_{off}	0 W
$P_{on \to off}$	10 W
$P_{off \to on}$	40 W
$t_{on \to off}$	1 s
$t_{off \to on}$	2 s
t_R	25 s

Policy	Energy	Avg. Latency
Always on	250 J	1 s
Reactive greedy	240 J	3 s
Power-aware	140 J	2.5 s

DYNAMIC OPERATION MODES

- Memory Access

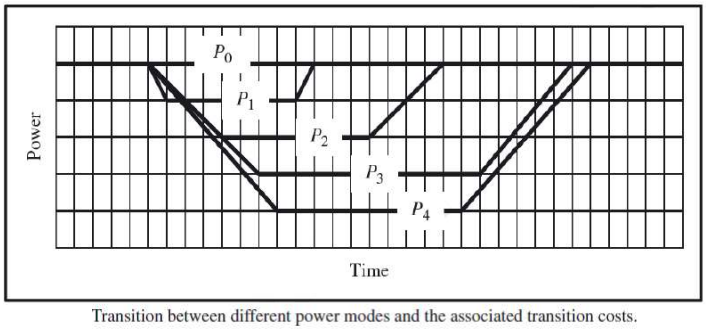


Power Mode	StrongARM	Memory	MEMS & ADC	RF
P_0	Sleep	Sleep	Off	Off
P_1	Sleep	Sleep	On	Off
P_2	Sleep	Sleep	On	RX
P_3	Idle	Sleep	On	RX
P_4	Active	Active	On	TX, RX

DYNAMIC OPERATION MODES

Power saving configurations

Configuration	Processor	Memory	Sensing subsystem	Communication subsystem
P_0	Active	Active	On	Transmitting/receiving
P_1	Active	On	On	On (transmitting)
P_2	Idle	On	On	Receiving
P_3	Sleep	On	On	Receiving
P_4	Sleep	Off	On	Off
P_5	Sleep	Off	Off	Off



Transition between different power modes and the associated transition costs.

DYNAMIC OPERATION MODES

- The decision for a particular power mode depends on
  - The anticipated task in the queues of the different hardware components
- Failure to realistically estimate future tasks can cause a node to miss interesting events or to delay in response
- In a WSN, the events outside of the network cannot be modeled as deterministic phenomena
  - e.g., a leak in a pipeline; a pestilence in a farm
  - No need for setting up a monitoring system
- An accurate event arrival model enables a DPM strategy to decide for the right configuration that has a *long duration* and *minimal power consumption*

DYNAMIC OPERATION MODES

Transition Cost

Suppose:

- Each subsystem of a wireless sensor node operates in just two different power modes only, it can be either *on* or *off.*
- Moreover, assume that the transition from *on* to *off* does not have an associated power cost
- But the reverse transition (from *off* to *on*) has a cost in terms both of power and a time delay.
- These costs are justified if the power it saves in the *off* state is large enough.
- In other words, the amount of the *off* state power is considerably large and the duration of the *off* state is long
- It is useful to quantify these costs and to set up a transition threshold

DYNAMIC OPERATION MODES

Transition Cost

Suppose:

- The minimum time that a subsystem stays in an *off* state is *t*off
- The power consumed during this time is *P*off
- The transition time is *t*off,on
- The power consumed during the transition is *p*off,on
- The power consumed in an *on* state is *P*on. Hence:

$$P_{\text{off}} \cdot t_{\text{off}} + P_{\text{off,on}} \cdot t_{\text{off,on}} \geq P_{\text{on}} \cdot \left(t_{\text{off}} + t_{\text{off,on}}\right) \quad \text{..... Eq. 1}$$

- Therefore, *t*off is justified if:

$$t_{\text{off}} \geq \max\left(0, \frac{\left(P_{\text{on}} - P_{\text{off,on}}\right) \cdot t_{\text{off,on}}}{P_{\text{on}} - P_{\text{off}}}\right) \quad \text{..... Eq. 2}$$

DYNAMIC OPERATION MODES

Transition Cost

Equations 1 and 2 can describe a subsystem with *n* distinct operational power modes

- In this case a transition from any state *i* into *j* is described as *ti,j*
- Hence, the transition is justified if Equation 3 is satisfied

$$t_j \geq \max\left(0, \frac{\left(P_i - P_{j,k}\right) t_{i,j}}{P_i - P_j}\right) \quad \text{..... Eq. 3}$$

where *tj* is the duration of the subsystem in state *j*